CLAIMS

We claim:

1. A synchronizing data protocol for use in synchronizing timing between a master device and a codec, comprising:

a preamble insertion module in said master timing device adapted to insert a preamble code word into selected frames in a data stream for transmission to said codec; and

a synchronizing preamble detection module in said codec device adapted to detect a presence of said preamble code word in said data stream.

2. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 1, wherein:

said selected frames are non-contiguous.

3. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 1, wherein:

a timing in said codec is synchronized based on a timing of a detection of said preamble code word in said data stream.

4. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 1, further comprising:

control address and data information adapted for transmission with said preamble code word, said control address and data information relating to system parameters in said codec.

5. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 1, further comprising:

an interrupt module having an operation based on an alteration of a clock signal from said master device to said codec.

6. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 5, wherein said interrupt module comprises:

a first clock absence timer in said codec adapted to detect an absence of said clock signal for at least a predetermined length of time.

7. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 6, wherein said interrupt module further comprises:

a second clock absence timer in said master device to provide an indication of said predetermined length of time to said master device.

8. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 5, wherein:

said alteration of said clock signal is a non-changing clock signal for at least a predetermined length of time.

9. The synchronizing data protocol for use in synchronizing timing between a master device and a codec according to claim 1, further comprising:

a buffer in said codec adapted to be enabled upon detection of said preamble code word.

sub a2 10. A method of synchronizing a codec to a serial data bus, said method comprising:

providing an interrupt signal to said codec;

monitoring a data stream received by said codec for a presence of a synchronizing preamble code word; and

basing a timing in said codec on a timing of a detection of said synchronizing preamble code word by said codec.

11. The method of synchronizing a codec to a master device over a serial data bus according to claim 10, wherein said providing step comprises:

halting a transmission of a clock signal over said serial data bus for at least a predetermined length of time.

sub a3 12. The method of synchronizing a codec to a master device over a serial data bus according to claim 10, wherein:

said synchronization is performed occasionally with respect to a frame signal.

13. The method of synchronizing a codec to a master device over a serial data bus according to claim 11, wherein:

said predetermined length of time is at least 25 microseconds.

14. Apparatus for synchronizing a codec to a master device over a serial data bus, said method comprising:

means for providing an interrupt signal to said codec;

means for monitoring a data stream received by said codec for a presence of a synchronizing preamble code word; and

means for basing a timing in said codec on a timing of a detection of said synchronizing preamble code word by said codec.

15. The apparatus for synchronizing a codec to a master device over a serial data bus according to claim 14, wherein said means for providing said interrupt signal comprises:

means for halting transmission of a clock signal over said serial data bus for at least a predetermined length of time.

16. The apparatus for synchronizing a codec to a master device over a serial data bus according to claim 14, wherein:

said synchronization is performed occasionally with respect to a frame signal.

17. The apparatus for synchronizing a codec to a master device over a serial data bus according to claim 15, wherein:

said predetermined length of time is at least 25 microseconds.